AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the

application:

LISTING OF CLAIMS:

1. (canceled).

2. (currently amended): A managing method for a re-order buffer in an out-of-order execution

processor for predicting the flow of a program by branch prediction, determining a next

executable instruction from an instruction string in the program and speculatively executing the

instruction based on ~~the basis of~~ a dependence relationship between the prediction and the

instruction, in which said re-order buffer rewrites an execution result according to a program

order and the end of the instruction is notified from each of a plurality of ~~unction~~ function units

containing a branching unit and a load unit to said re-order buffer by using a WRB number

corresponding to an entry number of said re-order buffer, which comprises the steps of:

managing ~~the~~ a latest speculation state of a load instruction issued to said load unit by

said load unit based on ~~the basis of~~ a branch prediction success/failure signal output from said

branching unit and suppressing notification to said re-order buffer by said load unit, as to a

subsequent load instruction of a branch instruction for which the ~~branching~~ branch prediction has

failed, based on ~~the basis of~~ the WRB number of the subsequent load instruction even if the

processing of the load instruction ~~concerned~~ issued to said load unit is finished, and

re-using an entry stored with the subsequent load instruction of the branching instruction

for which the branching branch-prediction has failed, by the re-order buffer, to store a new

instruction before the end notification based on the WRB number of the entry concerned is

received,

wherein a control signal for discriminating non-speculative execution/speculative

execution for every instruction under consideration, which corresponds to a branching level, is

generated in an instruction fetch/decode unit, the branching level being set to zero when the an

instruction concerned under consideration is an instruction for non-speculative execution, and the

branching level being set at a value of 1 or more which is determined by the number of

branching instructions interposed between the an instruction for the non-speculative execution

and the an instruction for the speculative execution when the an instruction concerned under

consideration is an instruction for speculative execution, the control signal thus generated is held

in said re-order buffer and said load unit, and the branching level is decremented by 1 in said re-

order buffer and said load unit when a branch-prediction failure signal is output from said

branching unit, thereby managing the latest instruction speculation state.

3. (currently amended): The managing method as claimed in claim 2, wherein said load unit has

plural entries, each of which holds a load instruction issued to said load unit together with the

branching level and the WRB number thereof, and wherein the entries having a branching level

of 1 or more are set to a cancel state when a branch-prediction failure signal is output from said

branching unit, and with respect to load instructions held in the entries under the cancel state, a

notification to the re-order buffer based on the basis of the WRB numbers of the load instructions

~~concerned~~ issued to said load unit is suppressed even if the processing of the load instructions

issued to said load unit is finished.

4. (canceled).

5. (currently amended): An out-of-order execution processor for predicting the flow of a

program by branch prediction, determining a next executable instruction from an instruction

string in the program and speculatively executing the instruction based on ~~the basis of~~ a

dependence relationship between the prediction and the instruction, in which a re-order buffer in

said processor rewrites an execution result according to a program order and the end of the

instruction is notified from each of a plurality of function units containing a branching unit and a

load unit to said re-order buffer by using a WRB number corresponding to an entry number of

said re-order buffer, which comprises:

managing means for managing ~~the~~ a latest speculation state of a load instruction issued to

said load unit based on ~~the basis of~~ a branch prediction success/failure signal output from said

branching unit and suppressing notification to said re-order buffer, as to a subsequent load

instruction of a branch instruction for which the ~~branching~~ branch prediction has failed, based on

~~the basis of~~ the WRB number of the subsequent load instruction even if the processing of the

load instruction ~~concerned~~ issued to said load unit is finished, said managing means being

contained in said load unit, wherein the re-order buffer re-uses an entry stored with the

subsequent load instruction of the branching instruction for which the ~~branching~~ branch

prediction has failed, to store a new instruction before the end notification based on the WRB

number of the entry concerned is received,

wherein a control signal for discriminating non-speculative execution/speculative

execution for every instruction under consideration, which corresponds to a branching level, is

generated in an instruction fetch/decode unit, the branching level being set to zero when ~~the~~ an

instruction ~~concerned~~ under consideration is an instruction for non-speculative execution, and the

branching level being set at a value of 1 or more which is determined by the number of

branching instructions interposed between ~~the~~ an instruction for the non-speculative execution

and ~~the~~ an instruction for the speculative execution when ~~the~~ an instruction ~~concerned~~ under

consideration is an instruction for speculative execution, the control signal thus generated is held

in said re-order buffer and said managing means, and the branching level is decremented by 1 in

said re-order buffer and said managing means when a branch-prediction failure signal is output

from said branching unit, thereby managing the latest instruction speculation state.

6. (currently amended): The processor as claimed in claim 5, wherein said managing means has

plural entries, each of which holds a load instruction issued to said load unit together with the

branching level and the WRB number thereof, and wherein the entries having a branching level

of 1 or more are set to a cancel state when a branch-prediction failure signal is output from said

branching unit, and with respect to load instructions held in the entries under the cancel state, a

notification to the re-order buffer based on ~~the basis of~~ the WRB numbers of the load instructions

~~concerned~~ issued to said load unit is suppressed even if the processing of the load instructions

issued to said load unit is finished.

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